

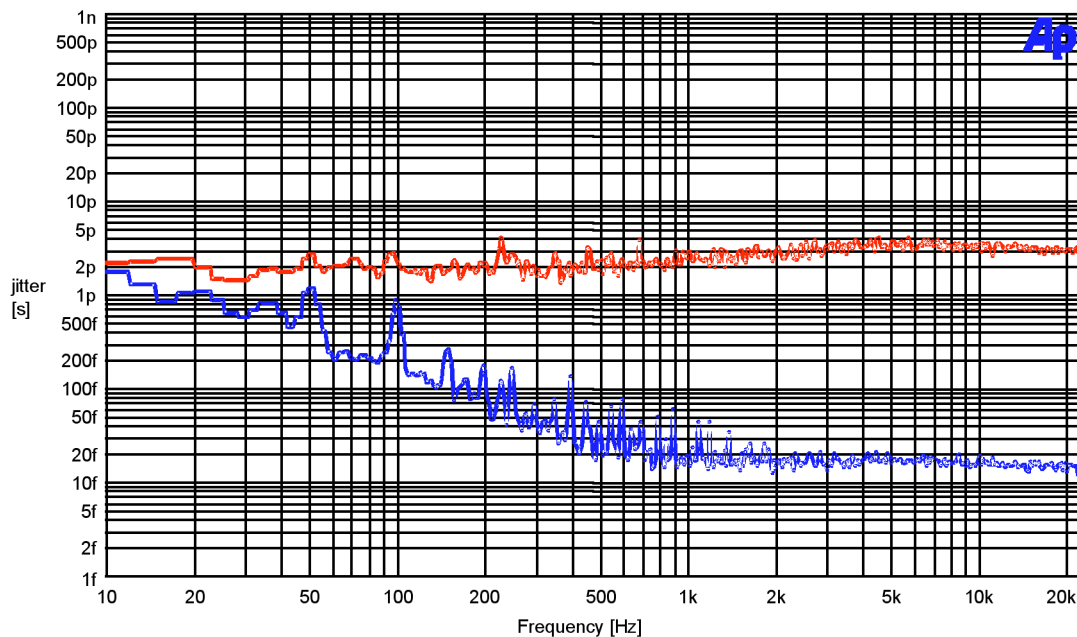
SFD-2 MkIII Jumper Configurations

The SFD-2 MkIII has adjustable settings through jumpers for single or dual phase lock loop (**J201**), level of dither (**J301**, **J302**), and HDCD gain on or off (**J303**). These are described below. Additional jumper configurations are specific to SFD-2 type – 3-input version with toggle switch selector, or 5-input version with pushbutton selector. **J601** is factory-set according to version. For the 3-input version, **J602** can be adjusted to make either the coaxial (COAX) or AT&T glass optic (ST) input active. For the 5-input version, J602 must remain in the COAX position. To connect a BNC cable to the coaxial input, use an RCA to BNC adapter.

To make any changes to the jumper configuration, pull the jumper (the small black square that surrounds two of three pins) upwards, and slide it down into the new position.

Two PLLs for Maximum Jitter Attenuation (J201)

The CS8414 input receiver is the first phase lock loop (PLL). The CS8414 will accept 16-bit to 24-bit/32 kHz to 96 kHz digital audio signals. The second stage is a discrete PLL with custom made voltage controlled crystal oscillators (VCXO). This proprietary circuit is where the jitter attenuation really occurs. Imagine this, just .02 ps (picoseconds) of absolute jitter, from 1 kHz and up! (see figure below). RMS output jitter is less than 2 ps broad band. Two VCXOs are used to decode the four most popular clock frequencies---44.1 kHz and 88.2 kHz with one VCXO, and 48 kHz and 96 kHz with the other VCXO. The SFD-2 MkIII will also accept an input sampling rate of 32 kHz, but the output signal will be without the strengths of the second PLL in terms of jitter attenuation.



The intrinsic jitter is shown for the first PLL (top trace), and the second PLL (bottom trace). The RMS values are 150 ps and 2 ps, respectively.

When J201 is set to 'D' (double PLL), the Lock LED will come on when the second PLL is engaged. This may take up to 20 seconds. If the second PLL does not engage, then the transport being used has a sampling rate error of more than 200 ppm (parts per million), and J201 should be set to 'S' (single PLL).

Selectable Dither Levels for Optimum Converter Performance (J301, J302)

Four levels of HDCD noise-shaped dither can be added to both standard and HDCD signals. Resolution is lost when low-level signals are recorded since only the least significant bits are used. Dither is used to reduce the errors, and to extend the dynamic range of the system. The amount of added dither is a matter of personal preference. Modes 1 through 4 have increasing levels of HDCD high-frequency dither, as do modes 5 through 8.

HDCD Level (J303)

When J303 is set to 0 (modes 1 through 4), HDCD operates at a level 6 dB higher than standard signals. To make both HDCD and standard signals have the same level, set J303 to 1 (modes 5 through 8).

